Remarks:

Applicant appreciatively acknowledges the Examiner's confirmation of receipt of applicant's claim for priority under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application is requested.

Claims 1 to 13 remain in the application. Claims 1, 4, 9, and 10 have been amended.

In items 1 and 2 on pages 2 to 3 of the above-identified Office action, the Examiner objected to claims 1 and 9 because of various informalities. It is respectfully believed that the amendments to claims 1 and 9 as set forth below remove any objectionable matter.

In item 5 on pages 3 to 8 of the above-identified Office action, claims 1 to 13 have been rejected as being obvious over Lepejian et al. (U.S. 6,085,346; hereinafter "Lepejian") under 35 U.S.C. § 103.

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page

13, line 20, to page 14, line 19, of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1, as amended, calls for, *inter alia*, a circuit for testing a data memory, including:

a comparison device:

connected to a processing device and to a data memory;

receiving test data from the data memory; and

determining if the data memory is faulty based upon a comparison of the test data items produced by the processing device and the stored data items read from the data memory.

Claim 9, as amended, calls for, *inter alia*, a method of testing a data memory including the step of:

detecting a fault in the data memory by comparing a plurality of the test data items with one another.

Claim 1 now includes a comparison device that receives a number of test data from the data memory on which the second function has been applied and compares the received test data items with one another. As set forth in claim 4, a fault signal is output to a fault signal line as soon as there is a difference between at least one of the received test data items and the others. Claim 9 detects a fault in the data memory by a comparison of the test data items. Claim 10 includes a step similar to the comparison features of claim 1.

Lepejian discloses a memory device having a BIST circuit. The BIST circuit includes a data comparator that compares the test data written into the memory under test and the test data read out of the memory under test. As a result, a fault signal is generated. Lepejian does not disclose the comparator or comparison of amended claims 1 or 9.

The main difference between the comparison device of the present invention and the Lepejian comparison device is that, in the present invention, several test data read out of the memory are applied to the second function and are, afterwards, compared to each other. The test data read out of the memory under test indicated in Lepejian are compared to the test data (decoded data) that were written into the memory under test

*beforehand*. In Lepejian, the test data are not multiplied in number ("a number of the data items being greater than a number of test data items") by a respective first function and a comparison of the test data with each other after read-out is not possible. Therefore, there is neither a motivation nor a suggestion for a person skilled in the art to provide a comparison device as used in the present invention.

Clearly, Lepejian does not show a circuit or a method as recited in claims 1 or 9 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 9. Claims 1 and 9 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 9.

In view of the foregoing, reconsideration and allowance of claims 1 to 13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Applic. No. 09/977,787
Response Dated June 24, 2004
Responsive to Office Action of March 24, 2004

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicant

Gregory L. Mayback
Reg. No. 40,719

GLM:kf

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101